

## THE BERKELEY SETI PROGRAM: SERENDIP III AND IV INSTRUMENTATION

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**ABSTRACT** The SERENDIP program is an ongoing search for narrow band radio signals from extraterrestrial civilizations. In this paper we discuss the hardware design of the SERENDIP III and IV instruments.

### INTRODUCTION

SERENDIP III is a four million channel FFT-based spectrum analyzer that has been operating in a sky survey mode at NAIC's 305 m radio telescope in Arecibo, Puerto Rico since April, 1992. The spectrum analyzer covers a 2.5 MHz instantaneous bandwidth with 0.6 Hz resolution.

SERENDIP IV is the next generation of SERENDIP instruments, which we hope to deploy in mid-1995. Building on the SERENDIP III design, SERENDIP IV is a 167 million channel spectrum analyzer, covering a 96 MHz bandwidth. It also has 0.6 Hz resolution and a 1.7 second integration time. SERENDIP IV incorporates a bank of digital mixers and filters to separate the 96 MHz band into forty 2.4 MHz sub-bands. Each 2.4 MHz sub-band is further broken down into 0.6 Hz bins by means of a four million point fast Fourier Transform. The resulting power spectra are analyzed by 40 high speed signal processors. Narrow band signals having power significantly above background noise levels are recorded, along with telescope coordinates, time, and frequency. The data are then sent to Berkeley for subsequent analysis and appropriate follow up observations.

### SERENDIP HARDWARE – PAST AND FUTURE

The tremendous growth rate in SETI instrumentation is illustrated in Figure 1. The first generation SERENDIP instrument had 100 channels (Bowyer *et al.* 1983); it was surpassed a few years later by SERENDIP II's 65,536 channels (Werthimer *et al.* 1984). Thereafter it was quickly eclipsed

by the 4,194,304 channel SERENDIP III machine, which will be followed by the 167,772,160 channel SERENDIP IV in 1995. Each generation SERENDIP instrument has, on average, been about 35 times more powerful than its predecessor, with a growth factor of about 2.7 per year. This growth rate is higher than that of any industry, even surpassing the growth in computer speed or weaponry capabilities. This growth is driven largely by the commercial development of digital signal processing and the availability of inexpensive FFT and high density dynamic RAM chips.

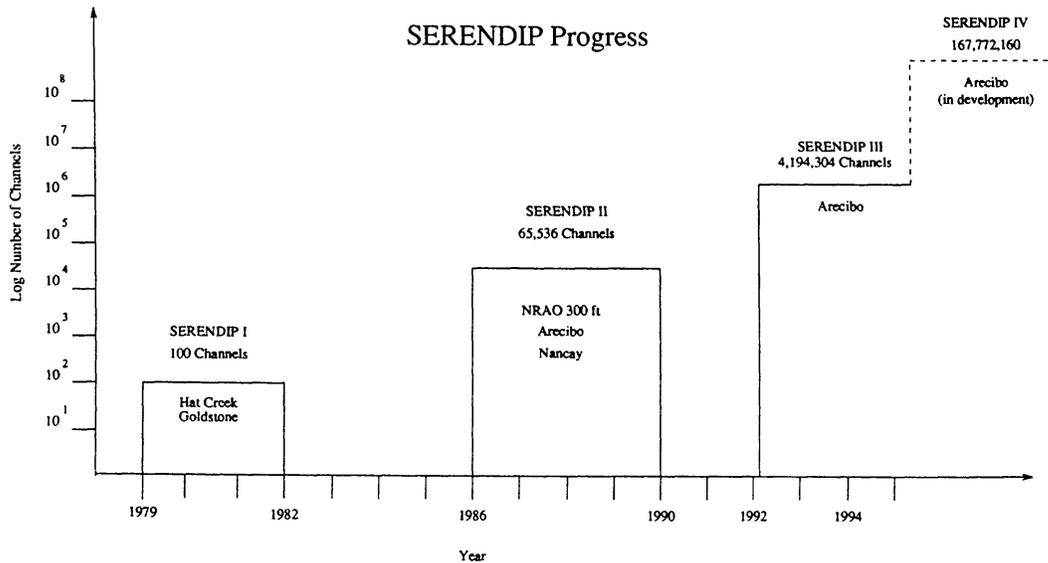


Figure 1. The number of channels in SERENDIP instrumentation increases by a factor of 2.7 every year.

These rapid technological improvements make it worthwhile to spend a considerable fraction of total effort in SETI developing new instrumentation, since observations with new equipment usually catch up to the previous generation's observations in a few weeks.

It will be interesting to see if this growth rate can be maintained. There are no physical constraints that limit the speed and scale of electronics until another factor of 1 million is reached (when gates will be the size of protein molecules). However, the current generation SETI instrumentation is already close to analyzing the total bandwidth available from typical radio telescope receivers. After this limit is reached, the growth rate can only continue by building very wide bandwidth receivers, or conducting the search at higher frequencies (where wide bandwidth receivers become easier to build), or by developing multiple beam radio telescopes (Dixon, this volume).

During this million-fold increase in the capabilities of SERENDIP instrumentation, the size of the instrument has remained roughly constant.

All generations of SERENDIP have fit into a few suitcases; they have been relatively easy to check onto flights to observatories. Also during this factor of a million increase, the development effort for a new generation instrument has remained constant – a few person-years of software and hardware.

About half of our instrumentation efforts go into hardware – the balance goes into software for both real time data acquisition and off-line data analysis (Donnelly *et al.*, this volume). This paper will concentrate on the hardware design of SERENDIP III and IV.

### SERENDIP III

SERENDIP III is a real-time, 4,194,304 channel fast Fourier Transform-based spectrum analyzer. Each channel is 0.6 Hz wide, yielding a total instantaneous bandwidth coverage of 2.5 MHz in a 1.7 second integration time. SERENDIP III has been operating continuously at NAIC's Arecibo Observatory since April 15, 1992. Almost all observations have utilized the telescope's 430 MHz (70 cm) receiver.

Although the 70 cm wavelength is not one of the traditional bands for SETI observations, it has several advantages. The 430 MHz receiver has by far the highest gain of all the Arecibo receivers (averaging about  $15 \text{ K Jy}^{-1}$ ) providing a sensitivity of  $4 \cdot 10^{-25} \text{ W m}^{-2}$ . The long wavelength provides a wide beam, allowing us to cover the sky quickly (every 6 months). Although some additional noise is contributed by synchrotron radiation at this low frequency, this noise does not contribute substantially to the overall system temperature. The 430 MHz band has not been explored by any other SETI effort to date.

The hardware consists of four major components (see Figure 2): the front end electronics, the FFT board, the post-processor board, and the data logging and system-management host computer.

The front-end system converts a 2.5 MHz portion of the intermediate frequency (IF) signal to baseband, and digitizes it for processing by the FFT board. Figure 3 shows a block diagram of the front-end system. Before digitizing, the IF signal is fed through an automatic gain control (AGC) amplifier to maintain a constant power level. Power levels are also monitored and logged by the SERENDIP host computer. The IF signal is then split into quadrature components by a pair of mixers. The down-mix frequency comes from a low phase noise programmable frequency synthesizer (Wavetek 5130A) and a quadrature phase splitter. For accurate frequency generation, the synthesizer is phase locked to the observatory's maser. After each integration period, the host computer steps the down-mix frequency by 2.4 MHz cyclically scanning the entire 12 MHz IF band every 8.4 seconds.

The quadrature baseband signals from the mixers are sent through a carefully matched pair of 1.23 MHz nine pole Cauer elliptic low-pass filters, and digitized by a pair of six-bit flash analog to digital converters (ADCs). Four bits from each ADC are utilized by the FFT board. Studies show that four bit quantization introduces only a 1% degradation in signal-to-noise ratio for signals dominated by noise. To enhance image rejection, special

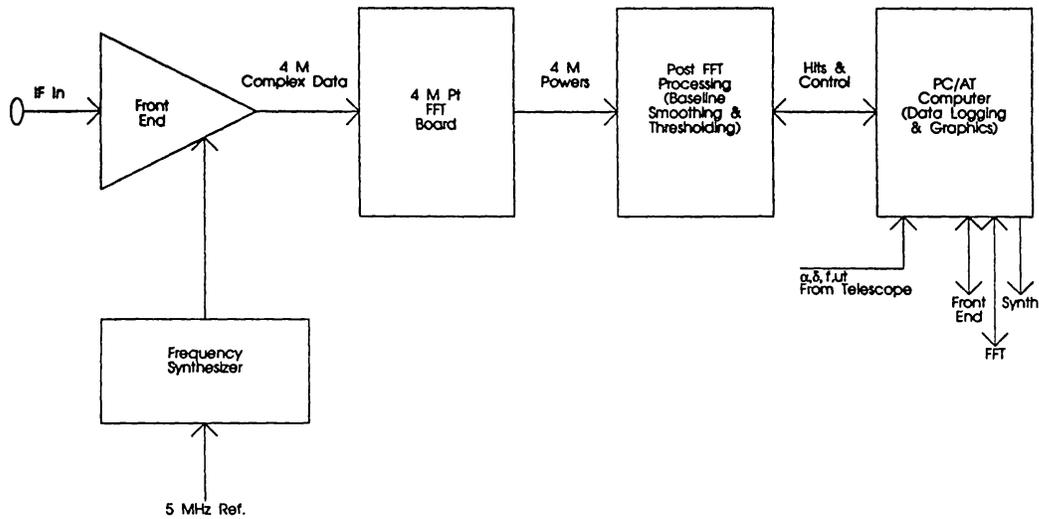


Figure 2. Block Diagram of SERENDIP III.

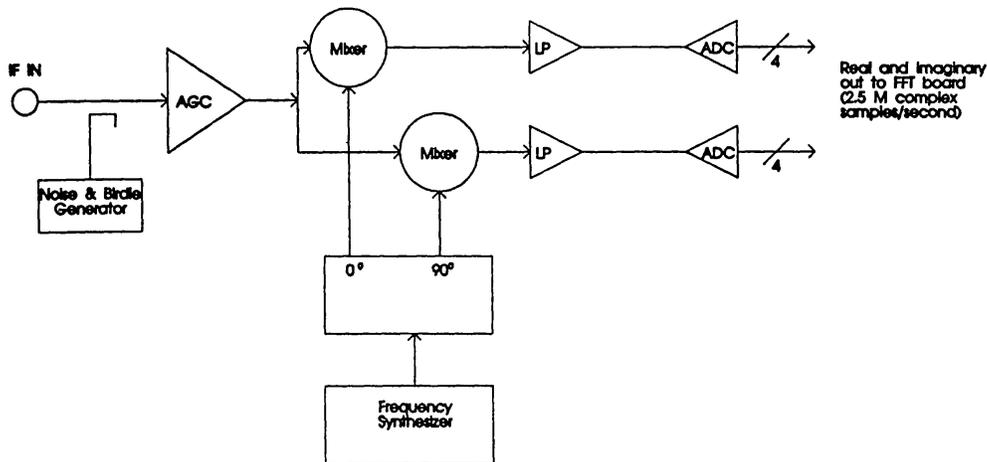


Figure 3. Block Diagram of the SERENDIP III Front End Downconverter.

attention was given to phase and amplitude matching of the low pass filters and power splitters.

A programmable “birdie generator” and wide-band noise source are built into the front-end electronics for system testing and calibration. As a test mechanism, the birdie generator injects a weak narrow-band signal through a directional coupler into the IF band to simulate an extraterrestrial transmission. This signal is left on during all observations as a constant test of the system.

Data pass from the front end system to the FFT processing board. The FFT board computes a four-million point Fourier Transform every

1.68 seconds on the complex input signal. The frequency resolution of the Fourier power spectrum is 0.596 Hz for a total band coverage of 2.5 MHz. In real time, the FFT board executes about 1,000 million instructions per second (MIPS), computing large FFTs an order of magnitude faster than the Cray XMP supercomputer, yet the parts cost of the FFT board is only \$3,000 (less than 0.1 cents per channel).

The FFT board is based on four Austek A41102 FFT chips selected in 1989 after extensive review of several chip manufacturers including Austek, Plessey, TRW, and Zoran. The Austek chips are no longer fabricated by Austek, but are now produced and sold by AWA Microelectronics. Each chip can compute FFTs up to 256 points in length and can perform calculations with 16, 20 or 24 bit precision. We chose the 16 bit mode in our design to save memory costs and improve speed. The 16 bit arithmetic provides sufficient dynamic range (16 bits of real and 16 bits of imaginary yield 32 bits of power), but we have had to be careful to scale the vectors at various stages throughout the computation.

In the SERENDIP III FFT board (Figure 4), the four-million point transformation is computed as a square 2048 by 2048 point FFT with the appropriate roots of unity (twiddle factors) multiplied with each data element between the column and row operations. The 2048-point transforms are similarly computed as 64 by 32 point square FFTs with twiddle-factor multiplies between the column and row operations. We conducted extensive computer simulations of this technique in order to verify our algorithms and architecture, and also to analyze the degradation effects of finite precision arithmetic. We find no significant degradation, and are able to detect weak signals in the presence of strong RFI.

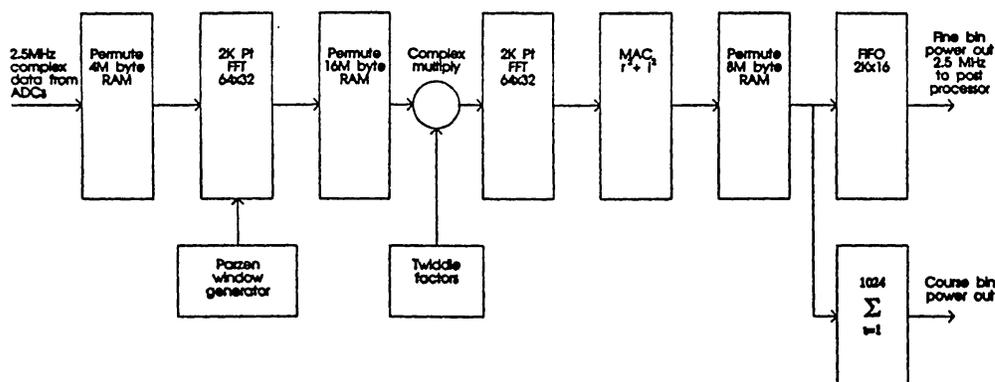


Figure 4. Block Diagram of the Serendip III FFT Board.

Almost all of the addressing, control, and “glue logic” for the FFT board has been designed into four Xilinx 3042 programmable gate array chips. Each chip contains the equivalent of 4,200 gates; the gate arrays are configured by SERENDIP’s host computer during the power up sequence. For testing and debugging, the gate arrays can be reconfigured and programmed to inject test patterns at almost any place in the FFT board data flow.

On the FFT board, the complex samples from the ADC’s are first re-ordered by a four mega-sample address permuter transforming the data in 2048 point segments. The samples are then multiplied by a Parzen window to increase sensitivity to narrow-band signals falling between adjacent spectral bins. Next, 2048 2K-point FFTs are performed by two Austek chips and associated circuitry. The resulting data is re-ordered by another permuter and multiplied by the twiddle factors. After the twiddle-factor multiply operation, another set of 2048 2K-point transforms is computed. Finally, the power spectrum is calculated from the complex data set by a multiplier-accumulator chip, and the data are unscrambled by a final permuter into a frequency ordered spectrum. Each of the three 4 million point permutes are done in a single DRAM buffer, which is automatically refreshed by means of clever address mapping. The entire FFT operation is computed in 1.68 seconds; however, the pipeline architecture produces a latency through the whole FFT board of about five seconds.

The FFT board also computes local averages of the power spectrum for each 1024 points and delays the spectral data by 4096 points to make the post processor addressing simpler. This hardware addition eases the computation load off the post processor.

The SERENDIP III post processing system is based on an Intel EV80960CA evaluation board driven by an 80960-CA microprocessor operating at 33 MHz and executing instructions at a sustained rate of about 45 MIPS. The high processing rate of the i80960-CA is needed to support a continued real-time throughput and analysis of the 2.5 million point per second 16-bit power spectrum from the FFT board. The post processing board performs the baseline normalization and searches for peaks above the threshold (the threshold for the narrow resolution bins is usually set to around 16 times the mean power). To improve sensitivity to wider bandwidth signals (*e.g.*, modulated signals), the post processor also forms coarse resolution spectra by adding adjacent bins together and performs threshold operations on spectra with successively coarser binwidths of 0.6, 1.2, 2.4, 5, 10, 20, 40, 80, ....., up to 640 Hz.

Data logging, control, and system synchronization is conducted by an 80386 PC. The computer logs information on strong signals along with coordinate and frequency information from the observatory computer, as well as controlling the front-end, FFT board, and post processor. Besides interfacing to the the FFT board and post processor board, the computer receives time code information every millisecond via a custom designed IRIG receiver board and receives the telescope’s azimuth and zenith angle every

10 seconds via an RS232 link. The PC controls the front end frequency synthesizer and frequency counter over an IEEE488 link and utilizes an ethernet transceiver to transmit its data and receive new parameters, software, and commands.

## SERENDIP IV

SERENDIP IV, a 167,772,160 million channel spectrum analyzer, is the next generation of SERENDIP instruments. We are constructing the instrument now, and expect to have it operating at Arecibo in mid-1995. Building on the SERENDIP III design, SERENDIP IV contains a bank of 40 SERENDIP III-like FFT boards. When combined together, these boards cover a 96 MHz bandwidth at 0.6 Hz resolution and a 1.7 second integration time. Since the system is modular, it can be split up in two sections to process two polarizations of 48 MHz each. Alternatively, it can be split into two or four separate instruments in order to process signals from separate antennas.

SERENDIP IV first utilizes conventional analog mixers and filters to break the band down into 36 MHz pieces. A block diagram of the system is shown in Figure 5. Each 36 MHz band is then further broken down into fifteen 2.4 MHz sub-bands by a bank of digital mixers and filters. Finally, each 2.4 MHz sub-band is further broken down into 0.6 Hz bins by means of a four million point fast Fourier Transform similar to that used in the SERENDIP III system.

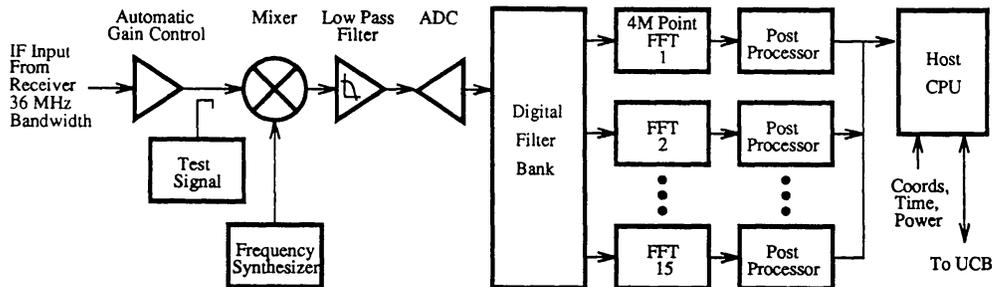


Figure 5. Block Diagram of a 60 million channel section of SERENDIP IV.

A block diagram of SERENDIP IV's digital filter board is shown in Figure 6. The complex digital down mix is performed by a high speed SRAM lookup table. The digital low pass filters employed are 256-tap FIR filters (Harris HSP43168) which also decimate the data by 16. The digital filter bank provides very low phase noise, excellent image rejection and very sharp filter cutoffs. Each digital filter board can drive eight

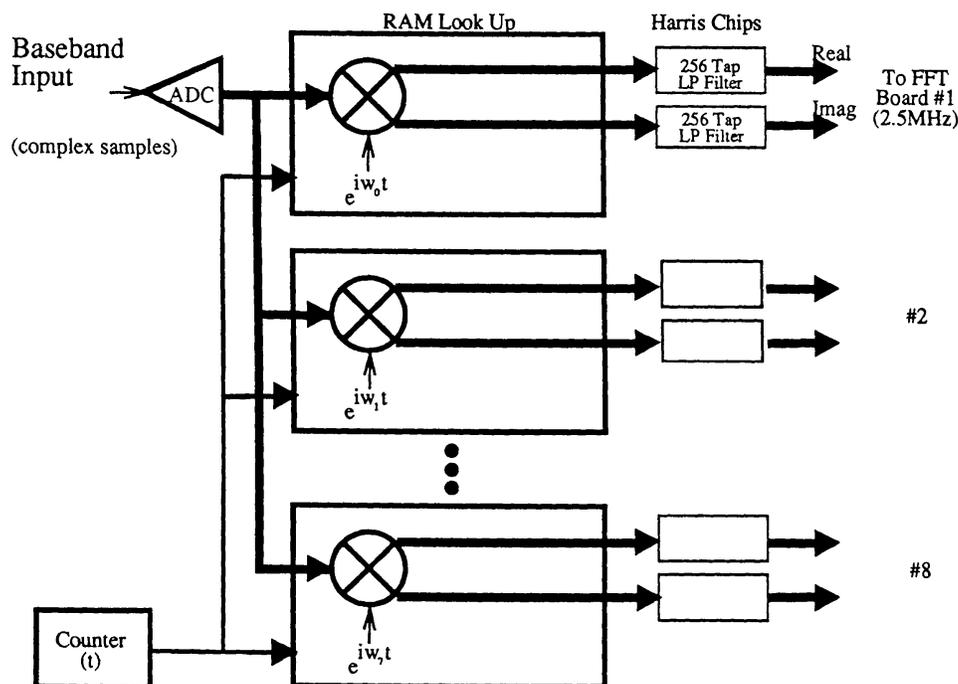


Figure 6. Block Diagram of the SERENDIP IV Digital Filter Bank Board.

FFT-postprocessor boards. The digital filter board can also generate test patterns to test itself and the subsequent FFT-postprocessor boards.

SERENDIP IV's FFT boards are very similar to those used in SERENDIP III, except that we added the postprocessor onboard, and instead of decomposing the  $2^{22}$  point FFT into 64:32:64:32 point transforms, it is broken up into 128:128:256 point transforms. We also used larger (and thus fewer) Xilinx gate arrays.

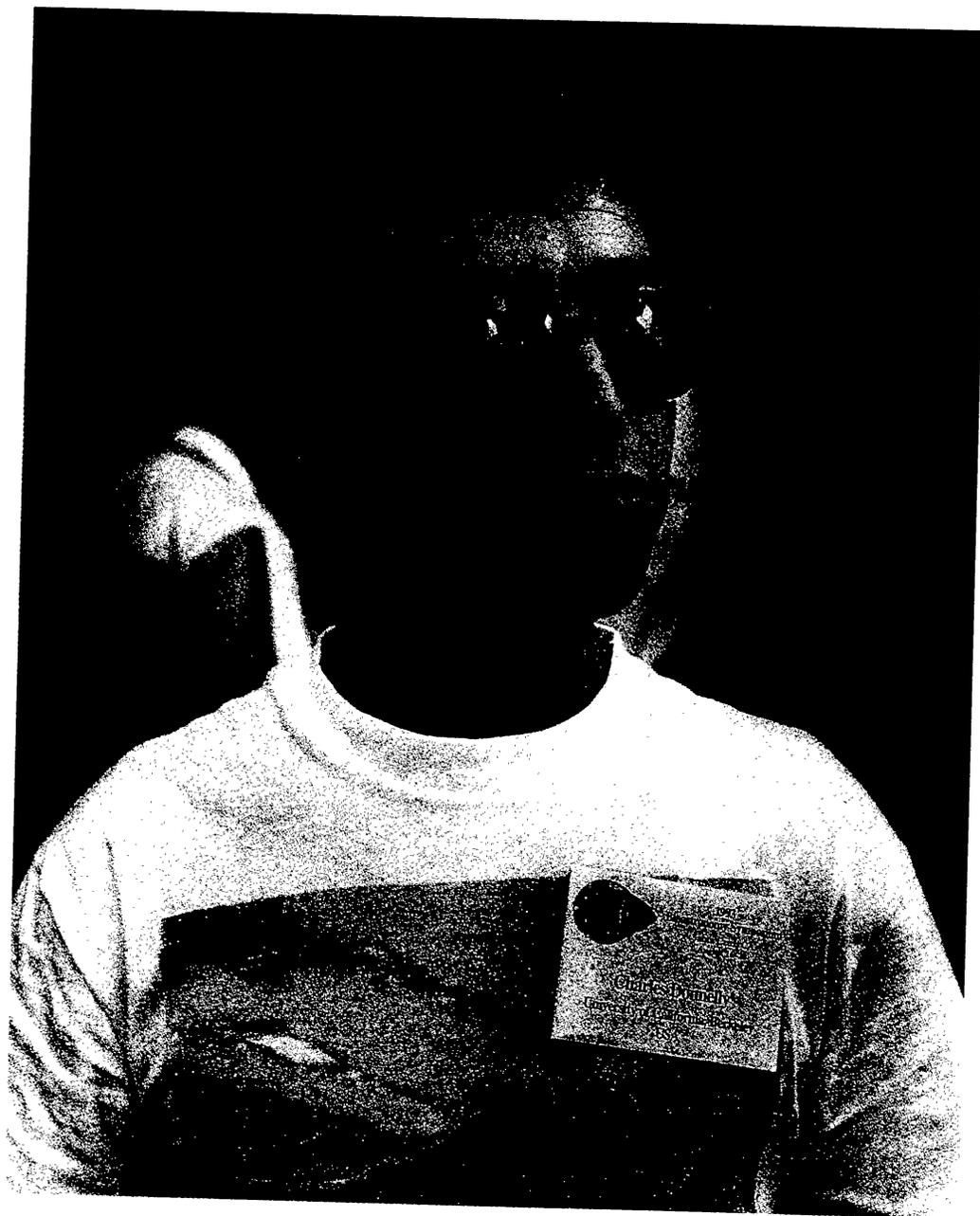
Perhaps the highest compliment to SERENDIP has come from other SETI researcher's utilization of SERENDIP designs and instruments. NASA used a SERENDIP II system for RFI studies and preliminary SETI searches. The SERENDIP III/IV FFT design was adopted for the Harvard/Planetary Society's BETA project. BETA will replace the current META systems now used at Harvard and Argentina. The SERENDIP IV digital filter boards are utilized by the pulsar timing program at Berkeley and will soon used for a pulsar search at the Naval Research Labs. Additionally, we are currently building a 4 million channel system for the Ohio State University SETI program (author's note: this system is now up and running at the OSU Radio Observatory).

### ACKNOWLEDGEMENTS

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*Chuck Donnelly refuses to accept everything.*